The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor active layer is a polycrystal semiconductor film;

wherein a grain boundary of a crystal grain in the polycrystal semiconductor film is flat or formed with a recessed portion; and

wherein a surface roughness of the channel region is 0.1 nm through 60 nm in a P-V value.

2. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor active layer is a polycrystal semiconductor film constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a grain boundary of the crystal grain constituting the polycrystal semiconductor film is flat or formed with a recessed portion.

3. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the channel region is a polycrystal semiconductor film crystallized by being irradiated with a continuously oscillating laser beam at least in the same channel region; and

wherein a surface roughness of the channel region is 0.1 nm through 60 nm in a P-V value.

4. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode;

wherein the semiconductor memory element is formed over a substrate having an insulating surface,

wherein the semiconductor active layer is a polycrystal semiconductor film constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a surface roughness of the channel region is 0.1 nm through 60 nm in a P-V value.

5. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type

impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the channel region is a polycrystal semiconductor film crystallized by being irradiated with a continuously oscillating laser beam at least in the same channel region; and

wherein a surface roughness of the channel region is 0.1 nm through 5 nm in an rms value.

6. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor active layer is a polycrystal semiconductor film constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a surface roughness of the channel region is 0.1 nm through 5 nm in an rms value.

7. (Canceled)

8. (Previously Presented) The semiconductor memory element according any one of claim 1 through claim 6, wherein the semiconductor active layer is the polycrystal semiconductor film subjected to a heating treatment and adding a metal element.

9. (Previously Presented) The semiconductor memory element according to claim 8, wherein the metal element is one kind or a plurality of kinds selected from the group consisting of Fe, Ni, Co, Ge, Sn, Pd, Pt, Cu, and Au.

10. (Previously Presented) The semiconductor memory element according to any one of claim 1 through claim 6, wherein a channel length of the semiconductor memory element is 0.01 μm through 2 μm.

11. (Previously Presented) A semiconductor memory device, further including a memory cell array arranged with the semiconductor memory element according to any one of claim 1 through claim 6 in a shape of a matrix.

12. (Previously Presented) A semiconductor memory device, wherein a memory cell array arranged with the semiconductor memory element according to any one of claim 1 through claim 6 in a shape of a matrix is formed on a plastic substrate or a ceramic substrate.

13. (Previously Presented) A semiconductor memory device, including an IC chip constituted by laminating a nonvolatile memory having a memory cell array arranged with the semiconductor memory element according to any one of claim 1 through claim 6 in a shape of a matrix.

14. (Previously Presented) A semiconductor memory device, wherein the semiconductor memory device according to any one of claim 1 through claim 6 is one selected from a game machine, a video camera, a head attaching type display, a DVD player, a personal computer, a portable telephone, and a car audio.

15.-16. (Canceled)

17. (Currently Amended) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

~~wherein the channel region is a crystallized polycrystal semiconductor film;~~

wherein the semiconductor active layer is a crystallized polycrystal semiconductor film;

wherein the semiconductor active layer is constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a grain boundary of a crystal grain in the polycrystal semiconductor film is flat or formed with a recessed portion.

18. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the channel region is a crystallized polycrystal semiconductor film; and

wherein a surface roughness of the channel region is 0.1 nm through 60 nm in a P-V value.

19. (Previously Presented) A semiconductor memory element comprising a semiconductor active layer comprising a channel region and one conductive type

impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the channel region is a crystallized polycrystal semiconductor film; and

wherein a surface roughness of the channel region is 0.1 nm through 5 nm in an rms value.

20. (Canceled)

21. (Previously Presented) The semiconductor memory element according any one of claim 17 through claim 19, wherein the semiconductor active layer is the crystallized polycrystal semiconductor film subjected to a heating treatment and adding a metal element.

22. (Previously Presented) The semiconductor memory element according to claim 21, wherein the metal element is one kind or a plurality of kinds selected from the group consisting of Fe, Ni, Co, Ge, Sn, Pd, Pt, Cu, and Au.

23. (Previously Presented) The semiconductor memory element according to any one of claim 17 through claim 19, wherein a channel length of the semiconductor memory element is 0.01 μm through 2 μm.

24. (Previously Presented) A semiconductor memory device, further including a memory cell array arranged with the semiconductor memory element according to any one of claim 17 through claim 19 in a shape of a matrix.

25. (Previously Presented) A semiconductor memory device, wherein a memory cell array arranged with the semiconductor memory element according to any one of claim 17 through claim 19 in a shape of a matrix is formed on a plastic substrate or a ceramic substrate.

26. (Previously Presented) A semiconductor memory device, including an IC chip constituted by laminating a nonvolatile memory having a memory cell array arranged with the semiconductor memory element according to any one of claim 17 through claim 19 in a shape of a matrix.

27. (Previously Presented) A semiconductor memory device, wherein the semiconductor memory device according to any one of claim 17 through claim 19 is one selected from a game machine, a video camera, a head attaching type display, a DVD player, a personal computer, a portable telephone, and a car audio.